REMARKS

This is in response to the Office Action mailed on July 1, 2004, and the references cited therewith.

Claims 1, 4-5, 8-9 and 13-14 are amended, and claims 19-22 are added; as a result, claims 1-22 are now pending in this application.

§*103 Rejection of the Claims*

Claims 1-18 were rejected under 35 USC § 103(a) as being unpatentable over Ozeki et al. (U.S. 5,402,385) in view of Helmbold et al. (U.S. 5,497,450) and Kimura (U.S. 5,625,593).

The invention claimed herein solves a problem of providing a method for write protecting flash memory devices in a way such that they are suitable for use in the gaming industry. Such flash memory devices are desirable for a variety of reasons including convenient packaging, lack of moving parts and low costs. However, data stored in such devices may be altered, which could result in adverse consequences in a gaming industry application. To avoid such a possibility, many jurisdictions have rules that either require that the gaming control program is contained in a storage medium that is not alterable or place additional constraints on gaming control programs that do not exist in such protected storage mediums. For example, the New Mexico Gaming Control Board regulations § 15.1.7.10(A) requires that: "Except as otherwise authorized by the board, the gaming device control program must reside in the gaming device that is contained in a storage medium that is not alterable through use of the circuitry or programming of the gaming device itself."

The system claimed herein meets the requirements of such regulations by adding a logic circuit that has an output connected to the write enable bit of the memory card. The logic circuit uses the same address bits used to specify the protected data registers as inputs. If these inputs are set to specify an address of the protected data registers, the logic circuit outputs a signal to the write enable bit of the memory card, disabling the write function. Thus, there is no way to alter the selected data registers using the circuitry or programming of the device it is installed on once installed.

Modification would require that the hardware of the memory card be altered. This is a critical difference between the claimed invention and the cited prior art, Ozeki et al. and Helmbold et al. Each prior art reference allows the selected registers of the installed memory card to be altered using the circuitry or programming of the device if the user knows a password. Ozeki et al. disclose that such a password consists of signals applied to unassigned address bits, "writing of data into the memory 1 is prohibited if the value on the address line 8 is different from the specific value." Col. 5, lines 27-29. Helmbold et al. describe a user interface for disabling the write protection, "the memory protection circuit 36 is disabled by a password followed by simultaneous actuation of particular keys of the keyboard 26 with the keyboard interface controller 40 in a write protection disable mode." Col. 8, lines 41-44. Kimura allows the same modifications, without a password, as long as the power supply is properly connected to the installed memory card.

These references describe methods and devices that have features that are contrary to what is claimed herein which is that modification of selected data registers requires that hardware of the memory card be altered. Furthermore, the references cited herein do not describe devices that are acceptable for use in the gaming industry because they permit alteration of a gaming control program that is contained in a storage medium and do not place additional constraints on gaming control programs.

The claimed invention, unlike the cited references, both complies with requirements of various statutes and regulations common in the gaming industry and improves the security and integrity of gaming control programs.

The claims, as amended, also include decoding a selected address of the storage medium. The Examiner suggests that Ozeki et al. describes this element of the claim because "the external terminals A20 to A25 for transmitting the upper bits of the address from the external device are connected to the decoder of the gate circuit." Col. 5, lines 50-53. The address lines in the Ozeki et al. reference are not the same as the address lines described by Applicant. Ozeki et al. describe using address lines that are unassigned. The abstract states, "existing address lines exceeding the capacity of a memory and an existing write control line are used as inputs to a gate circuit." Thus, though the inputs A20 to A25 are labeled as address lines, they do not function as such because the memory space is completely defined by the actual

address lines A0 to A19. In contrast, Applicant teaches connecting the same address lines that are used to locate a space in the memory to a logic circuit so that specific data registers are protected. Ozeki et al. describe an identical concept applied to a different standard on page 6, line 34 to page 7, line 4. There, A22 to A25 are the unassigned bits that require a specific decode value in order to allow writing of data. Thus, Ozeki et al. do not teach decoding a selected address of the storage medium as described by Applicant.

The amended claims include disabling one load condition and also disabling more than one load condition. The Examiner admits that Ozeki et al. does not disclose disabling more than one load condition, but states that Kimura discloses disabling more than one load condition. The Examiner cites, "Normally, when the SRAM's 2a to 2n are not accessed, the chip enable signal CE, the write enable signal WE and the output enable signal OE are all in an inactive state, namely, at "H" level." Col. 6, lines 55-58. This reference merely describes the common operation of a memory card. The chip enable, write enable and output enable signals are not described as being disabled, only inactive. The load conditions are clearly not disabled, as Kimura describes the process of reading and writing data to the memory card in great detail at col. 6, line 66 through col. 7, line 25. Thus, none of the references disclose disabling more than one load condition.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6976 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 30th day of September, 2004.

Peter Rebuffoni
Name

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